PCT WORLD INTELLECTUAL PROPERTY ORGANIZATION
International Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 5 :
H01L 39/22, B05D 5/12

A1

(11) International Publication Number: WO 92/05591

(43) International Publication Date: 2 April 1992 (02.04.92)

(21) International Application Number: PCT/US91/06812

(22) International Filing Date: 19 September 1991 (19.09.91)

(30) Priority data:
586,435 21 September 1990 (21.09.90) US

(71) Applicant: THE REGENTS OF THE UNIVERSITY OF CALIFORNIA [US/US]; 300 Lakeside Drive, 22nd Floor, Oakland, CA 94612-3550 (US).

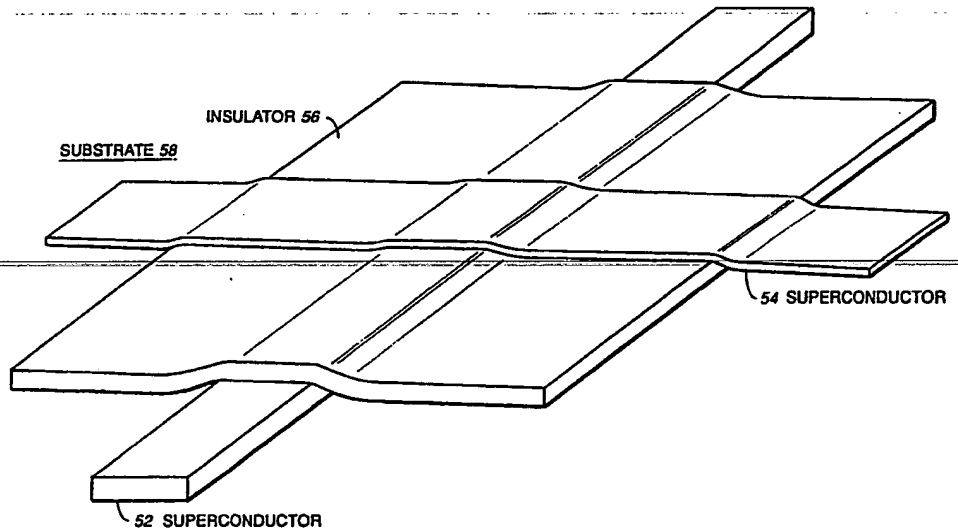
(72) Inventors: WELLSTOOD, Frederick, C. ; 1221 A University, Berkeley, CA 94702 (US). KINGSTON, John, J. ; 77 Yosemite Avenue, Oakland, CA 94611 (US). CLARKE, John ; 657 Cragmont, Berkeley, CA 94708 (US).

(74) Agents: McCUBBREY, J., Bruce et al.; McCubbrey, Bartels, Meyer & Ward, Suite 2700, One Post Street, San Francisco, CA 94104-5231 (US).

(81) Designated States: AT (European patent), BE (European patent), CH (European patent), DE (European patent), DK (European patent), ES (European patent), FR (European patent), GB (European patent), GR (European patent), IT (European patent), JP, LU (European patent), NL (European patent), SE (European patent).

Published
With international search report.

(54) Title: IMPROVED MICROELECTRONIC SUPERCONDUCTING DEVICES AND METHODS



(57) Abstract

A microelectronic component comprising a crossover is provided comprising a substrate (58), a first high T_c superconductor thin film (52), a second insulating thin film (56) comprising $SrTiO_3$; and a third high T_c superconducting film (54) which has strips which crossover one or more areas f the first superconductor film. An in situ method for depositing all three films on a substrate is provided which does not require annealing steps. The photolithographic process is used to separately pattern the high T_c superconductor thin films.

FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	ES	Spain	MG	Madagascar
AU	Australia	FI	Finland	ML	Mali
BB	Barbados	FR	France	MN	Mongolia
BE	Belgium	GA	Gabon	MR	Mauritania
BF	Burkina Faso	GB	United Kingdom	MW	Malawi
BG	Bulgaria	GN	Guinea	NL	Netherlands
BJ	Benin	GR	Greece	NO	Norway
BR	Brazil	HU	Hungary	PL	Poland
CA	Canada	IT	Italy	RO	Romania
CF	Central African Republic	JP	Japan	SD	Sudan
CG	Congo	KP	Democratic People's Republic of Korea	SE	Sweden
CH	Switzerland			SN	Senegal
CI	Côte d'Ivoire	KR	Republic of Korea	SU+	Soviet Union
CM	Cameroon	LI	Liechtenstein	TD	Chad
CS	Czechoslovakia	LK	Sri Lanka	TG	Togo
DE*	Germany	LU	Luxembourg	US	United States of America
DK	Denmark	MC	Monaco		

+ Any designation of "SU" has effect in the Russian Federation. It is not yet known whether any such designation has effect in other States of the former Soviet Union.

IMPROVED MICROELECTRONIC SUPERCONDUCTING DEVICES AND METHODS

This invention relates to electrical structures comprised of high transition temperature (T_c) superconductor materials. More particularly, the invention relates to microelectronic superconductor devices and an improved method for making such devices wherein the superconductor material has a high transition temperature. This application contains subject matter supported by the U.S. Government under Contract No. DE-AC03-76SF00098, through the U.S. Department of Energy. The government has certain rights in this invention.

Superconductor materials have been developed which have a high transition temperature (T_c), exhibiting superconductivity at temperatures up to and above the boiling point of liquid nitrogen, 77K. The ability to manufacture microelectronic devices employing high T_c superconducting material promises many advantages. Such devices exhibit the advantages of devices employing low temperature superconducting material, but because they can operate in liquid N_2, they can be cooled much more easily and less expensively.

Unfortunately, the fabrication of microelectronic structures using high T_c superconductor materials is not a trivial task, and cannot readily follow prior art techniques. For example, low T_c superconductor materials, such as niobium and niobium nitride, may be fabricated using conventional techniques such as vacuum evaporation deposition, sputtering, reactive ion etching, and photolithographic patterning techniques. Examples of microelectronic structures using low temperature superconductor materials are described by Klepner in IEEE Transactions on Magnetics, January, 1981, pp. 282 et. seq., by Jaycox, et al. in the same publication at pp. 400 t. seq., by Nagasawa, et al. in IEEE Transactions on Magnetics, March 1989, pp. 777 et. seq., and by

Kaplunenko, et al. in the same publication at pp. 861, et seq.

Such common fabrication techniques are not readily suited to many types of multilayer microelectronic devices employing high T_c superconductor materials. The reasons for this involve the fact that, in order to be superconducting, high T_c materials must have the correct crystal structure. The correct crystal structure can be achieved using an annealing step at a high temperature, for example, 850°C, after the material is deposited. However, thin films of high T_c superconductor materials are highly defected and, at such annealing temperatures, will interdiffuse rapidly with adjacent layers. Since many microelectronic structures require multiple layers of different materials, an annealing step is not practical. Thus, a deposition technique which results directly in the formation of multiple heteroepitaxial layers is needed for the construction of such structures.

High T_c superconductor material may be deposited as epitaxial thin films on suitable substrates at temperatures between 650° and 750°C using laser deposition. In single layer microelectronic structures, a proper substrate surface will result in epitaxial thin films under suitable deposition conditions. However, where an insulating layer is required, such as in the case where conductors cross each other (crossover), it is difficult to achieve proper insulation and at the same time a crystal structure suitable for the deposition of a third epitaxial thin film layer.

Multilayer structures of high T_c superconductor material have been reported in a number of publications in connection with tri-layer junctions that exhibit Josephson Characteristics (superconducting pair tunneling). Examples of the tri-layer junctions are described by Rogers, et al. in Appl. Phys. Lett., Vol.

55, No. 19, November 6, 1989, pp. 2032 et. seq., by Iguchi, et al. in Japanese Journal of Applied Physics, Vol. 29, No. 4, April, 1990, pp. L614 et. seq., by Ienari, et al. in Second ISTEC Workshop on Superconductivity, May 28-30, 1990, pp. 125 et. seq., and by Furuyama, et al. in Second Workshop on High Temperature Superconducting Electron Devices, June 7-9, 1989, pp. 105 et. seq. Such tri-layer structures are not suitable as cross-overs, however, since the intermediate layer has insufficient insulating properties for typical microelectronic crossover applications.

In addition to the need for providing insulation between high T_c superconductor layers, it is also necessary to pattern the high T_c superconducting layers and, in some cases, the insulating layer so that useful devices can be built. The use of photolithography on single and multilayer high T_c superconducting thin film structures is well known in the art as a patterning technique performed only after all high T_c superconducting films have been deposited. However, there would be a number of advantages in using the photolithographic process to separately pattern all layers of a multilayer high T_c superconducting thin film structure. First, the photolithographic process is the standard technique for patterning conventional microelectronic circuits. Thus, the use of the photolithographic process opens up the possibility of using existing standard equipment to produce novel superconducting devices. Second, photolithography allows the construction of complex patterns, while other prior art methods, such as patterned shadow masks, are generally suitable only for relatively simple patterns. Third, photolithography allows a given pattern to be exposed and stepped repeatedly over a film to produce a large number of identical devices on one substrate, thus allowing mass production of devices. Fourth,

photolithography also allows precise alignment of different layers. Finally, the photolithographic process allows the physical size of the patterns to be drastically reduced. Typically, the linewidths produced using the photolithographic process can be as small as a few micrometers. This is extremely important in many applications, in particular, where high speed is required or a large number of devices are to be put on a single chip.

Examples of devices which are best made using the photolithographic process are miniature muliturn coils and window contacts. A window contact is an area of electrical contact between two electrically conducting layers through a hole in an insulating layer. If the two layers are superconducting layers, a supercurrent, i.e., a current which does not encounter any electrical resistance, can flow from one superconductor layer to another superconductor layer through the hole in the insulating layer. The hole through the insulating layer is best patterned using the photolithographic process so that all the desirable advantages of using the photolithographic process described above can be realized.

The holes in the insulating layer have other applications in addition to providing window contacts. A plurality of layers can be deposited inside each hole. These layers inside the hole can be used to form superconductor-insulator-superconductor (SIS) and superconductor-normal-superconductor (SNS) junctions.

However, the ability to use the photolithographic process to separately pattern more than one high T_c superconducting thin film of a multilayer structure has not been achieved by the prior art. This is because the surface of a high T_c superconducting thin film becomes contaminated during the photolithographic process. Thus, it will not support the crystalline growth of an

insulating layer of sufficient quality that th insulating layer will, in turn, support the crystalline growth of a second high T_c superconducting thin film.

It is an object of the present invention to provide a multilayer high T_c microelectronic device with an insulating layer.

It is another object of the present invention to provide an improved method for manufacturing a microelectronic device employing high T_c superconductor material.

A further object of the invention is to use the photolithographic process to separately pattern thin films of high T_c superconductor materials and insulators in multilayer structures.

It is another object of the invention to facilitate mass production of microelectronic devices utilizing high T_c superconductor material.

A further object of the invention is to reduce the physical size of microelectronic devices employing high T_c superconductor material.

It is yet another object of the present invention to provide an improved method for producing a multilayer microelectronic device wherein two layers of high T_c superconductor materials are separated by an insulating layer.

It is still another object of the present invention to provide an improved method for producing window contacts in a multilayer microelectronic device employing high T_c superconductor material.

A further object of the present invention is to deposit a plurality of layers in the holes of the insulating layer.

These and other objects will become apparent from the following description, accompanying drawings, and from the practice of the invention.

SUMMARY OF THE INVENTION

The present invention provides a method to separately pattern more than one high T_c metal oxid superconductor film using the photolithographic process. The photolithographic process can be applied individually to all superconducting and insulating layers of superconductor film in a crossover or similar multilayer structure.

In a preferred embodiment, the method of the invention comprises depositing in situ a high T_c metal oxide superconductor film on a substrate at a temperature below 800°C. The deposited film is then patterned using the photolithographic process. The surface of the deposited film is then restored so as to support epitaxial or highly oriented microstructure in subsequent deposits. An insulating film is then deposited on at least part of said first film, said insulating film being comprised of a material having high resistivity at temperatures below T_c, and having a microstructure which is epitaxial or highly oriented sufficient to support epitaxial growth thereon of a third layer.

The present invention also provides a microelectronic device comprising a substrate and a first superconductor thin film of high T_c metal oxide superconductor material. The first superconducting thin film is covered by an insulating thin film having a plurality of holes. The insulating film comprises a material having high resistivity at temperatures below T_c, and has a microstructure which is epitaxial or highly oriented sufficient to support epitaxial growth thereon of a third layer.

DESCRIPTION OF THE FIGURES

FIGURE 1 is a perspective view of a portion of a crossover patterned using the photolithographic process.

FIGURES 2A and 2B are, respectively, a plan and side view of an example of a high T_c microelectronic crossover element constructed according to the present

invention.

FIGURES 3A-C are plots of resistance versus temperature of a photolithographically patterned crossover which is etched using nitric acid. Figure 3A is the resistance versus temperature plot of the upper YBCO layer. Figure 3B is the resistance versus temperature plot of the $SrTiO_3$ insulating layer measured between the upper and the lower YBCO layers. Figure 3C is the resistance versus temperature plot of the bottom YBCO layer.

FIGURES 4A-C are plots of resistance versus temperature of a photolithographically patterned crossover which is etched using an argon ion mill. Figure 4A is the resistance versus temperature plot of the upper YBCO layer. Figure 4B is the resistance versus temperature plot of the $SrTiO_3$ insulating layer measured between the upper and the lower YBCO layers. Figure 4C is the resistance versus temperature plot of the bottom YBCO layer.

FIGURE 5A and 5B are, respectively, a plan and cross sectional view of an example of a device with a window contact constructed according to the present invention.

FIGURE 6 shows resistance versus temperature data for a window contact with all the layers patterned photolithographically according to the present invention.

FIGURE 7 shows the critical current versus temperature for the window contact in Figure 6.

FIGURE 8 shows a hole with multiple layers deposited within according to the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Methods are known in the art for the deposition of single layers of thin films of the class of high temperature superconductors know as ceramic oxides or metal oxides, of which the most well known is $YBa_2Cu_3O_x$ (x is a positive number up to 7.0), also known as YBCO

and sometimes referred to as 123 mixed metal oxide, based on the stoichiometric proportions of yttrium, barium and copper. However, to produce microelectronic circuits of any complexity, there is a need to develop techniques for depositing multilayer structures.

One important multilayer structure is an insulated crossover, which allows two thin film superconductors to overlap or to cross while maintaining electrical isolation. Virtually all electronic circuits of any complexity require such insulated crossovers. For example, one such utilization of a crossover is in the construction of a thin-film multi-turn superconductor coil. The crossover problem is encountered in making an electrical contact to the inner turn of the coil.

In addition to the electrical considerations, there are the additional problems associated with making a crossover structure using high T_c superconductor thin films. Most thin films are highly defected in nature and thus interdiffusion proceeds much more rapidly than in a single crystal. If the as-deposited film does not have the correct crystal structure, an annealing step is typically required to achieve the desired superconducting characteristics. For YBCO, the annealing temperature is typically about 850°C. However, at a temperature of 850°C, interdiffusion is so fast that a tri-layer structure which requires such a post-annealing temperature is probably impractical to fabricate. Therefore, to fabricate a tri-layer structure comprising mixed metal superconductor one needs to devise an in situ deposition process which is compatible with relatively low substrate temperature, short deposition time and a way to avoid high temperature annealing.

In order to employ high T_c ceramic oxide films for crossovers, the insulating layer should be able to grow epitaxially or in a highly orient d manner both on the substrate and on the ceramic oxide, as well as to

have good coverage of and adhesion to the ceramic oxide and the substrate, particularly at edges and over irregularities. It is also important that the insulating layer has a high resistivity and provides sufficient insulation between the upper and lower superconducting layers at temperatures below the transition temperature (T_c) of the ceramic oxide which is utilized in the device.

In addition to the need for an insulating layer, the high T_c ceramic oxide layers must be patterned in order to create microelectronic circuits. Patterning using photolithographic process has many advantages over prior art patterning methods. However, the insulating layer may not grow with the necessary crystal structure on the surface of a ceramic oxide thin film which has been contaminated during the photolithographic processing. In particular, YBCO is very reactive. It has been well documented that the surface of YBCO thin films can easily be contaminated even with exposure to air. Thus, the surface of the bottom YBCO film patterned photolithographically could be sufficiently contaminated so that it would not support growth of the insulating layer and the top YBCO layer with the necessary crystal structure. Defects in the structure of the insulating layer could result in short circuits between the two YBCO layers. In addition, defects in the crystalline structure of the upper YBCO layer could severely degrade the superconducting properties of the top YBCO layer, i.e., a reduction in superconducting transition temperature and/or a reduction in critical current.

There is another problem associated with using the photolithographic patterning technique which could also degrade the performance of the crossovers. When a film is patterned into lin s with this technique, the lines appears as rectangles when viewed in cross section. Referring now to Fig. 1 which shows a perspective view of

a portion of a crossover. A superconducting ceramic oxide film is photolithographically patterned into line 52 on top of a substrate 58. An insulating layer 56 is deposited so that another line 54 patterned from a top superconducting ceramic oxide film is insulated from line 52. The sides of the lines 52 patterned using photolithographic process is roughly perpendicular to the surface of the film. The rectangular geometry resulting from photolithographic processing makes it difficult to deposit an insulating layer which can sufficiently cover the corners of the bottom YBCO film so as to prevent short circuits. In addition, it is more difficult to deposit a top YBCO film with good superconducting properties upon this insulating layer because the top YBCO film has to climb over the "steps" created by line 52.

The present invention is based, in part, on the introduction of an additional step after the photolithographic process so that the problems of defects in epitaxial growth using the photolithographic process on high T_c ceramic oxide can be avoided. More specifically, the additional step involves restoring the surface of the bottom ceramic oxide layer after subjecting it to photolithographic patterning. Restoration is the removal of the contaminated surface layer of the film thereby leaving a surface suitable to support the epitaxial growth of subsequent layers.

The restoration step is preferably performed by submerging the substrate and the photographically patterned ceramic oxide film in a chemical etchant which is substantially free of water. This is because the surface of the YBCO layer can easily be contaminated by water. Thus, a chemical etchant which is substantially free of water can clean the surface to facilitate the deposition of other layers. An example of such chemical etchant is a mixture of bromine in methanol. The mixture

has been shown by others, such as Vasquet, et al., in Appl. Phys. Lett., December, 1988, pp. 2692 et. seq., to be able to restore the surface of YBCO and other high temperature superconductors.

The present invention is also based, in part, on the successful deposition of an insulating thin film layer which is thick enough to achieve sufficient insulation and to support the deposition of a third layer of either metal, such as gold or silver, another insulating layer or a high T_c superconducting material. This insulting layer can also be patterned using the photolithographic process.

A particularly desirable device which is best made using the photolithographic process on the insulating layer is a window contact. A window contact is an area of electrical contact through a hole in an insulating layer between a superconductor layer and another layer which can be either a metal or another superconducting layer. If the contact is between a lower ceramic oxide layer and an upper ceramic oxide layer, a supercurrent, i.e., a current which does not encounter any electrical resistance, can flow from one ceramic oxide layer to another ceramic oxide superconductor layer through the holes in the insulating layer. Contacts between a lower ceramic oxide layer and a metal can be used to make connections to normal metal circuitry.

Contacts between two conducting layers separated by an insulating layer have been made by the prior art at the edges of the insulating layer separating the two superconducting layers. The use of window contacts to provide electrical coupling between layers are superior to the methods used in the prior art because contacts can be made anywhere in the insulating layer. These holes are best fabricat d using photolithography to provide precision in alignment among the layers and reduction in the size of the holes. As a result, complicated

microelectronic devices can be fabricated.

In addition to allowing the use of photolithographic process on the lower ceramic oxide layer and the insulating layer, the present invention also allows the use of the photolithographic process on the top ceramic oxide layer. The application of the photolithographic process to the top ceramic oxide layer presents other problems. In particular, the use of a chemical etch, which is widely used in a typical photolithographic process involving only a single high T_c superconducting layer, could damage the lower ceramic oxide film if the insulating layer does not provide sufficient protection to the lower ceramic oxide film from chemical attack. In order to avoid the possibility of etching through the insulating layer, an Ar ion mill can be used instead of the chemical etch. In many instances, however, a chemical etch can be safely used. In addition, it has been found that the thickness of the insulating layer and the milling time should be well controlled so that the material underlying the top ceramic oxide layer is not damaged.

Accordingly, the present invention is directed to a process for making microelectronic devices wherein crossovers of superconductor metal oxides can be made and wherein the entire microelectronic device can be made without destroying the electrical properties of the materials which have already been deposited and which are to be deposited. The present invention is also directed to a multilayer device with one or more window contacts.

The thin films are deposited using a laser to ablate the targets, which are, preferably, stoichiometric YBCO, YSZ, or $SrTiO_3$ targets. The deposition can be done in a vacuum deposition chamber with the laser focused onto the target and with a substrate holder which can h at the substrate to the desired temperature. The substrate may be any suitable material, of which many are

known to those skilled in the art, such as MgO, $SrTiO_3$, YSZ, and $LaA10_3$. The substrate may also be materials which do not support the growth of high quality high T_c superconducting layers, such as silicon and sapphire wafers, but can be coated with materials which support such growth.

The substrate heater is first outgassed and the substrate temperature is raised to the range of about 650° to 750°C (for deposition, for example, of YBCO) while the deposition chamber is evacuated to about 2 to 5 μTorr. A preferred temperature for heating the substrate is about 730°C for YBCO. Oxygen is then bled into the system, since it is required to maintain proper stoichiometry in the deposited film. Typically, oxygen pressure within the vacuum chamber of about 150 to 250 mTorr, preferably about 190 mTorr, is useful for YBCO deposition.

Typically, prior to deposition, the target surface is cleaned with laser pulses and then the high T_c ceramic oxide, such as YBCO, is deposited by focusing the laser on a stoichiometric YBCO target formed by pressing and sintering calcined powder into disks. Preferably, the first layer is deposited to a thickness of about 0.1 to 0.6 μm (for YBCO layers); however the thickness may be varied depending on the final application and desired current carrying capacity of the microelectronic device. A thickness in the range of 0.2-0.4 μm is most preferred. After deposition, the chamber is filled with oxygen to about 700 Torr and the substrate block allowed to cool to about 450°C in about 15 minutes. After further cooling to a handleable temperature (about 100°C or less), the chamber may be opened and the substrate with the deposited ceramic oxide layer can be removed for patterning using the photolithographic process.

When using photolithography to pattern a thin film, the film is coated with an organic chemical called

photoresist. An example of a photoresist is Shipley Microposit 1400-31. The photoresist is baked dry, exposed to ultraviolet light in the desired pattern, and developed in an organic chemical developer such as Microposit developer so that a portion of the photoresist responsive to the ultraviolet light passing through the pattern is removed. The portion of the thin film which is not covered by the photoresist can then be etched away using either an ion mill or various chemical etchants. An example of a suitable etchant is dilute nitric acid. After etching is completed, the resist covering the remaining parts of the ceramic oxide film is stripped using acetone.

At this point, the surface of the ceramic oxide film is restored using a solution of bromine in methanol before depositing the final two layers. The concentration of the solution is preferably 2% bromine. The substrate with the ceramic oxide thin film is submerged in the restoring solution for preferably 30 seconds or less, then rinsed in pure methanol and blown dry. Immediately afterwards, it is mounted in the laser system's vacuum chamber in preparation for deposition of the insulating layer.

An appropriate evaporation mask, if desired, may be placed on top of the substrate. The vacuum chamber is closed and evacuated while the substrate is outgassed at about 200°C. This low temperature minimizes the loss of oxygen from the ceramic oxide layer. After the pressure within the chamber is lowered, preferably to about 3 to 5 μTorr, the substrate temperature is rapidly raised to a suitable temperature for deposition of the insulator, (about 680°C for $SrTiO_3$ deposition) and oxygen is bled in to obtain about 190 μTorr pressure. The target is cleaned with the laser, before a suitable insulator such as $SrTiO_3$, yttrium stabilized zirconia (YSZ), magnesium oxide (MgO), lanthanum aluminate ($LaAl_2O_3$), praseodymium

barium copper oxide ($PrBa_2Cu_3O_7$), or yttrium oxide (Y_2O_3) is deposited, preferably, for a period sufficient to form a 0.1 to 0.5 μm thick layer or such that it is sufficiently insulating. It is useful to use the same cooling, procedure as in the first deposition.

If it is desirable to pattern the insulating layer using the photolithographic process, the same procedure as described in patterning the lower YBCO layer can be used. However, it is found that a restoration step is not necessary for the insulating layer. It may be understood that the pattern which can be etched on the insulating layer includes holes, strips, and other desirable figures.

If it is desirable to create a beveled wall for the hole, one can defocus the projection mask aligner during exposure of the photo-resist. The insulating layer is etched using an ion milling. The defocused pattern allows some etching at the peripheral of the hole thereby forming a beveled wall. A hole with beveled wall is especially desirable for window contact. This is because the beveled wall provides a gentle slope to guide the third layer into the hole.

The third layer can either be metal, another insulating layer, or another YBCO layer. Metal can be deposited on the insulating layer using a thermal evaporation process, such process is well known in the art. The metal deposited can make contact with the lower YBCO layer through the holes etched in the insulating layer so that signals can be coupled to and from the lower YBCO layer.

If it is desirable to deposit YBCO as a third layer, the sample and a stoichiometric YBCO target is placed in the chamber. Outgassing and deposition may be accomplished as in the first deposition step. The third layer may us fully be deposited to a thickness of about 0.1 to 0.5 μm, if the layer is, for example, YBCO. The

third layer may be patterned by using a mask or by photolithography.

If the third layer is patterned using the photolithographic process, the same procedure as described in patterning the lower YBCO layer can be used with two modifications. First, in many instances, chemical etchants cannot be used in the etching step and one must use an ion mill. This is to protect the lower YBCO film from chemical attack by the acid. Second, there is no need for restoring the surface of the top YBCO film.

It may be understood that additional layers can also be deposited and patterned using the photolithographic methods described above.

Holes with beveled walls in the insulating layer are also useful for making superconductor-insulator-superconductor (SIS) and superconductor-normal-superconductor (SNS) junctions. After milling the defocused pattern to expose the underlying YBCO layer, a series of layers can be deposited inside each hole. The first layer of the series is preferably a thin YBCO layer designed to restore the surface of the underlying YBCO layer damaged during ion milling. An insulating layer or a normal metal layer could be deposited on top of the thin YBCO layer. A upper YBCO layer could be deposited on top of the intermediate insulating or normal metal layer. Upon patterning of the upper YBCO layer, a junction could be fabricated. A SIS junction could be produced if the intermediate layer is an insulating layer. A SNS junction could be produced if the intermediate layer is a normal metal layer.

Referring to Figure 8 there is shown a SNS or SIS junction according to the present invention. An insulating layer 73 with a beveled wall 75 is positioned above a lower YBCO thin film 72 forming a hole 77. Beveled wall 75 extends into lower YBCO film 72. A first

layer 74, pref rably YBCO, is deposited inside hole 77. A second layer 76, either a insulator or a normal metal, is deposited on top of first layer 74. A third layer 78, preferably YBCO, is deposited on top of second layer 76.

Referring to Figure 2 there is shown a microelectronic device having a high T_c superconductor crossover in accordance with the present invention. Referring to Figure 2A, a substrate 10 which is receptive to YBCO and $SrTiO_3$, is utilized. The preferred substrate is MgO having a polished surface. The first layer 11 comprises a strip metal oxide superconductor. The second layer 12 is insulating $SrTiO_3$ which, as shown, only partially covers the first layer and specifically only covers the portion of layer 11 where the crossover will occur. The third layer 13 comprises YBCO in the form of a strip that crosses over layer 11 where it is covered by layer 12.

Referring to Figure 2B, there is shown a side view of the device shown in 2A wherein the numerals 10, 11, 12, and 13 are as described above.

The following examples are provided by way of illustration and are not intended to limit the invention in any way.

EXAMPLE 1

A $12.5x12.5x1mm^3$ cleaved and polished (100) MgO substrate was cleaned successively in an ultrasonic bath with xylene, trichlorethylene, isopropyl alcohol and ethanol, rinsed with methanol, and blown dry with N_2. The superconductor films are deposited from stoichiometric YBCO targets pressed and sintered from calcined powder into disks 25 mm in diameter and 3 mm thick. The insulating layer is deposited from $SrTiO_3$ powder pressed into a disk of the same size. Before each deposition, the surface of the targets are ground with #400 emery paper, polished on a latex sheet and blown with N_2. Each layer is deposited in turn using the 248

nm pulses (18 ns full width at half maximum) from a Questek 2820 excimer laser. A 5.4 x 14mm² aperture selects the uniform portion of the beam, which is focused by a 0.15m focal length lens onto the target at an angle of incidence of 45°. The target is glued to one end of a copper cylinder that rotates at about 60 rpm; the bearings for the shaft are mounted in a water-cooled block in a diffusion-pumped vacuum system. The substrate is clamped to a heater block which is coated with a layer of silver paste to insure good thermal contact. This block is resistively heated, and its temperature is monitored by an embedded Chromel-Alumel thermocouple. The substrate is 60mm from the target, and aligned to intercept the central portion of the plume emanating from the target. A water-cooled plate partially shields the target from the thermal radiation emitted by the substrate heater block to prevent melting of the surface of the target.

The first step in the process is to outgas the heater and substrate by increasing the temperature to 740°C as the chamber is evacuated to 5 μTorr. Then, the temperature is held constant while the gate valve is throttled and 0_2 is bled in to maintain a pressure of 190 mTorr. The target is cleaned with 300 laser pulses at a rate of 5 per second with an energy density of $1.3Jcm^{-2}$. The first layer of YBCO is deposited for 6 minutes, at the same repetition rate and fluence, to a thickness of about 0.4 μm. The chamber is then back-filled with 0_2 to 1 atmosphere and the heater power is reduced to allow the block to cool to 450°C in about 15 minutes.

The sample is allowed to further cool down to 100°C or less in another 15 minutes. The sample is then dismounted from the heater block in preparation for patterning. Shipley Microposit 1400-31 photoresist is spun on the YBCO film for 30 sec at 5000 RPM and baked at 70°C for 5 minutes. This produces a 1/2 to 1 micrometer

thick layer of resist that entirely covers the YBCO film. The desired pattern is then exposed n the resist using a projection mask aligner. The resist is developed for 60 seconds using Microposit developer. The portion of the thin film which is not covered by the photoresist can then be etched away using either an ion mill or various chemical etchants. An example of a suitable etchant is dilute nitric acid.

When using nitric acid in etching, the sample is submerged in a 0.1% solution of nitric acid in water for about 45 seconds until the film is entirely etched in those regions where the resist has been removed by the developer. The substrate is then rinsed in water and blown dry.

When using an ion mill in etching, the substrate is clamped on a large copper block heat sink beneath an ion mill in a vacuum system. After evacuation is complete, argon (Ar) is bled into the system and a beam of Ar ions is used to etch away the chosen portions of the YBCO film. Typically, a 300nm thick film is milled for about 15 minutes in a 450V, 1.5 mA/cm^2 beam of Ar ions.

After etching is completed by either method, the resist covering the remaining parts of the YBCO film is stripped using ethanol or acetone in an ultrasonic bath. At this point, the surface of the YBCO film is restored by submerging the substrate in a solution of 2% bromine in methanol for 30 seconds. The sample is rinsed in pure methanol and then blown dry. Immediately afterwards, the sample is mounted in a laser system's vacuum chamber in preparation for deposition of the insulating layer.

An appropriate evaporation mask, if desired, may be is placed on top of the substrate and both are clamped to the heater block. The YBCO target is replaced with a polished $SrTiO_3$ target. As the chamber is evacuated to 3 μTorr, the heater block is outgassed at the relatively

low temperature of 200°C to minimize the loss of oxygen from the YBCO layer. The block temperature is then rapidly raised to 680°C, 0_2 is bled in to 190mTorr, and the target is cleaned as described above. After opening the shutter, $SrTiO_3$ is deposited for 8 minutes at a repetition rate of 4.8 Hz and a laser fluence of $1.3Jcm^{-2}$. The same cooling procedure is used.

After removing the evaporation mask and inserting a polished YBCO target, the substrate is outgassed at 200°C until the pressure falls to 3 μTorr. The temperature is quickly raised to 740°C and 0_2 is bled in to 200 mTorr. The third layer is deposited for 7 minutes at a repetition rate of 4.8 Hz and a laser fluence of 1.3 J/cm^2. After the usual cooling procedure, the sample is removed. This layer can also be patterned using either an evaporation mask or the photolithographic process used on the lower YBCO layer.

If it is desirable to pattern the top layer using the photolithographic process. Shipley Microposit 1400-31 photoresist is spun on the sample at 5000 RPM for 30 seconds, and then baked at 70°C for 5-7 min. This produces a 1/2-1 μm thick layer of resist. The pattern is then exposed, and the resist developed in microposit developer for approximately 60 seconds. The back of the sample is then coated with vacuum grease and clamped onto a large Cu block heat sink, and etched for a total of approximately 10 to 20 min in a 450 V, 1.5mA/cm² beam of Ar ions. To prevent heating damage to the YBCO, the milling can be done in intervals of 5 min with approximately 15 min cooling intervals between, and aluminum foil may be used to protect portions of the device that require less etching time. After milling, the photoresist is stripped off in 30 sec in an ultrasonic ethanol bath.

To reduce the particle density on the deposited YBCO film to typically 1 per 2500 μm², it is preferred

that the YBCO target face be polished before deposition, and that the laser pulse power/unit area be lowered to close to the minimum necessary to yield high quality films. A further reduction of particle density can be achieved by increasing the area of the target that is ablated by the laser, and/or by polishing the target face during deposition. The elimination, or at least the minimization of the density of 1 μm particles on the deposited film may be desirable in multilayer structures such as an insulated crossover, and is particularly important in a structure with a thin insulating layer such as a tunnel junction. The electrical properties of the three-layer component were measured using a 4-terminal arrangement, making contacts to the films with pressed Indium pellets.

Figures 3A-C show resistance versus temperature data of a crossover with its lower YBCO layer photolithographically patterned and etched using nitric acid (HNO_3). Figure 3A is of the resistance versus temperature plot of the upper YBCO layer. The transition temperature, T_c, is 87K. Figure 3B is the resistance versus temperature plot of the $SrTiO_3$ insulating layer measured between the upper and the lower YBCO layers. Figure 3C is the resistance versus temperature plot of the bottom YBCO layer. The transition temperature, T_c, is 84.7K.

Figures 4A-C show resistance versus temperature data of a crossover with its lower YBCO layer photolithographically patterned and etched using an ion mill. Figure 4A is the resistance versus temperature plot of the upper YBCO layer. The transition temperature, T_c, is 87K. Figure 4B is the resistance versus temperature plot of the $SrTiO_3$ insulating layer measured between the upper and the lower YBCO layers. Figure 4C is the resistanc versus t mperature plot of the bottom YBCO layer. The transition temperature, T_c,

is 86K.

EXAMPLE 2

A 12.5x12.5x1mm^3 cleaved and polished (100) MgO substrate was cleaned successively in an ultrasonic bath with xylene, trichlorethylene, isopropyl alcohol and ethanol, rinsed with methanol, and blown dry with N_2. The superconductor films are deposited from stoichiometric YBCO targets pressed and sintered from calcined powder into disks 25 mm in diameter and 3 mm thick. The insulating layer is deposited from $SrTiO_3$ powder pressed into a disk of the same size. Before each deposition, the surface of the targets are ground with #400 emery paper, polished on a latex sheet and blown with N_2. Each layer is deposited in turn using the 248 nm pulses (18 ns full width at half maximum) from a Questek 2820 excimer laser. A 5.4 x 14mm^2 aperture selects the uniform portion of the beam, which is focused by a 0.15m focal length lens onto the target at an angle of incidence of 45°. The target is glued to one end of a copper cylinder that rotates at about 60 rpm; the bearings for the shaft are mounted in a water-cooled block in a diffusion-pumped vacuum system. The substrate is clamped to a heater block which is coated with a layer of silver paste to insure good thermal contact. This block is resistively heated, and its temperature is monitored by an embedded Chromel-Alumel thermocouple. The substrate is 60mm from the target, and aligned to intercept the central portion of the plume emanating from the target. A water-cooled plate partially shields the target from the thermal radiation emitted by the substrate heater block to prevent melting of the surface of the target.

The first step in the process is to outgas the heater and substrate by increasing the temperature to 740°C as the chamber is evacuated to 5 μTorr. Then, the temperature is held constant while the gate valve is

throttled and 0_2 is bled in to maintain a pressure of 190 mTorr. The target is cleaned with 300 laser pulses at a rate of 5 per second with an energy density of $1.3Jcm^{-2}$. The first layer of YBCO is deposited for 5 minutes, at the same repetition rate and fluence, to a thickness of about 0.3 μm. The chamber is then back-filled with 0_2 to 1 atmosphere and the heater power is reduced to allow the block to cool to 450°C in about 15 minutes.

The sample is allowed to further cool down to 100°C or less in another 15 minutes. The sample is then dismounted from the heater block in preparation for patterning. Shipley Microposit 1400-31 photoresist is spun on the YBCO film for 30 sec at 5000 RPM and baked at 70°C for 5 minutes. This produces a 1/2 to 1 micrometer thick layer of resist that entirely covers the YBCO film. The desired pattern is then exposed on the resist using a projection mask aligner. The resist is developed for 60 seconds using Microposit developer. The portion of the thin film which is not covered by the photoresist can then be etched away using either an ion mill or various chemical etchants. An example of a suitable etchant is dilute nitric acid.

When using nitric acid in etching, the sample is submerged in a 0.1% solution of nitric acid in water for about 45 seconds until the film is entirely etched in those regions where the resist have been exposed. The substrate is then rinsed in water and blown dry.

When using an ion mill in etching, the substrate is clamped on a large copper block heat sink beneath an ion mill in a vacuum system. After evacuation is complete, argon (Ar) is bled into the system and a beam of Ar ions is used to etch away the chosen portions of the YBCO film. Typically, a 300nm thick film is milled for about 15 minutes in a 450V, 1.5 mA/cm^2 beam of Ar ions.

After etching is completed by either method, the

resist covering the remaining parts of the YBCO film is stripped using ethanol or acetone in an ultrasonic bath. At this point, the surface of the YBCO film is restored by submerging the substrate in a solution of 1% bromine in methanol for 10 seconds. The sample is rinsed in pure methanol and then blown dry. Immediately afterwards, the sample is mounted in a laser system's vacuum chamber in preparation for deposition of the insulating layer.

An appropriate evaporation mask, if desired, may be is placed on top of the substrate and both are clamped to the heater block. The YBCO target is replaced with a polished $SrTiO_3$ target. As the chamber is evacuated to 3 μTorr, the heater block is outgassed at the relatively low temperature of 200°C to minimize the loss of oxygen from the YBCO layer. The block temperature is then rapidly raised to 680°C, O_2 is bled in to 190mTorr, and the target is cleaned as described above. After opening the shutter, $SrTiO_3$ is deposited at a repetition rate of 4.8 Hz and a laser fluence of 1.3Jcm^{-2} so that the thickness of the $SrTiO_3$ is preferably between 0.1 to 0.4 μm. The same cooling procedure is used.

The sample is then dismounted from the heater block in preparation for patterning. Shipley Microposit 1400-31 photoresist is spun on the insulating layer for 30 sec at 2000 RPM and baked at 70°C for 6 to 7 minutes. This produces a 2 to 3 micrometer thick layer of resist that entirely covers the insulating layer. This relatively thick layer is necessary to withstand the long subsequent ion mill etch. The desired pattern, in this case, a hole, is then exposed on the resist using a Canon projection mask aligner. The aligner is defocused if it is desirable to create a hole with beveled wall. The resist is developed for 60 seconds using Microposit developer. The portion of the thin film which is not covered by the photoresist can then be etched away using an ion mill.

When using an ion mill in etching, the substrate is clamped on a large copper block heat sink beneath an ion mill in a vacuum system. After evacuation is complete, argon (Ar) is bled into the system and a beam of Ar ions is used to etch away the chosen portions of the insulating layer. Typically, a 300nm thick film is milled for about 30 minutes in a 600V, 1.5 mA/cm^2 beam of Ar ions. The last 3 to 5 minutes of the milling is preferably performed at 450V to reduce damage to the underlying YBCO layer.

After etching is completed, the resist covering the remaining parts of the insulating layer is stripped using ethanol or acetone in an ultrasonic bath. Immediately afterwards, the sample is mounted in a laser system's vacuum chamber in preparation for deposition of the third layer.

A polished YBCO target is inserted in the chamber and the sample is outgassed at 200°C until the pressure falls to 3 μTorr. The temperature is quickly raised to 740°C and 0_2 is bled in to 200 mTorr. The third layer is deposited at a repetition rate of 4.8 Hz and a laser fluence of 1.3 J/cm^2 so that the thickness of the third layer is preferably 0.3 to 0.4 μm. After the usual cooling procedure, the third layer is patterned using the photolithographic process.

Shipley Microposit 1400-31 photoresist is spun on the sample at 5000 RPM for 30 seconds, and then baked at 70°C for 5-7 min. The pattern is then exposed, and the resist developed in microposit developer for approximately 60 seconds. The back of the sample is then coated with vacuum grease and clamped onto a large Cu block heat sink, and etched for a total of approximately 10 to 20 min in a 450 V, 1.5mA/cm^2 beam of Ar ions. To prevent heating damage to the YBCO, the milling can be done in intervals of 5 min with approximately 15 min cooling intervals between, and aluminum foil may be used

to protect portions of the device that require less etching time. After milling, the photoresist is stripped off in 30 sec in an ultrasonic ethanol bath.

Fig. 5A-B show a microelectronic device with a window contact according to the present invention. Referring to fig. 5A, the microelectric device comprises a lower superconducting layer 31, an insulating layer 32 having a hole 34, and a upper superconducting layer 33. Fig. 5B is a cross-sectional view of the microelectronic device along a longitudinal direction parallel to lower superconducting layer 31 and including hole 34. Lower superconducting layer 31 and upper superconducting layer 33 make contact at location 35 thereby allowing electrical conduction between lower superconducting layer 31 and upper superconducting layer 33.

Fig. 6 shows resistance versus temperature data for a window contact of dimension 18 μm x 99 μm wherein all the layers are patterned photolithographically. The electrical contacts to the sample were made in such a way so as to include parts of the upper and lower YBCO stripes as well as the window contact in the resistance measurement.

FIG. 7 shows the critical current versus temperature for the 18 μm x 99 μm window contact.

The invention is described in terms of the preferred embodiments. It will be realized that other modifications and variations will be apparent from the above description and for practice of the invention to those skilled in the art. These modifications and variations are intended to be within the scope of the present invention and the invention is not intended to be limited except by the following appended claims.

WHAT IS CLAIMED IS:

1. A method for making a microelectronic device comprising

a. depositing a first film of high T_c metal oxide superconductor material on a substrate;

b. patterning said first film using a photolithographic process;

c. restoring the surface of said first film to support epitaxial or highly oriented microstructure in a material deposited thereon; and

d. depositing an insulating film on at least part of said first film, said insulating film being comprised of a material having high resistivity at temperatures below T_c, and having a microstructure which is epitaxial or highly oriented sufficient to support epitaxial growth thereon of a third layer.

2. A method according to Claim 1 wherein said step (b) comprises coating said first film with photoresist, exposing said photoresist with a desired pattern, developing said photoresist so that a portion of said photoresist responsive to said pattern is removed thereby uncovering a corresponding portion of said first film, and etching said uncovered portion of said first film.

3. A method according to Claim 1 wherein said restoring step comprises submerging said first film in a first chemical etchant which is substantially free of water for removing contamination from the surface of said first film.

4. A method according to Claim 3 wherein said first chemical etchant comprises a solution of bromine and methanol.

5. A method according to Claim 4 wherein said

solution comprises 1% to 2% bromine in methanol.

6. A method according to Claim 2 wherein said etching step comprises submerging said first film in a second chemical etchant for removing said uncovered portion of said first film.

7. A method according to Claim 2 wherein said etching step comprises milling said first film using an ion mill.

8. A method according to Claim 1 wherein said insulating film is selected from the group consisting of $SrTiO_3$, yttrium stabilized zirconia, magnesium oxide, lanthanum aluminate, praseodymium barium copper oxide, and yttrium oxide.

9. A method according to Claim 1 wherein said high T_c metal oxide superconductor film comprises a mixed metal oxide of yttrium, barium and copper.

10. A method according to Claim 1 which further comprises the step of patterning said insulating film using a photolithographic process.

11. A method according to Claim 10 wherein said step of patterning said insulating film comprises coating said insulating film with photoresist, exposing said photoresist with a desired pattern, developing said photoresist so that a portion of said photoresist responsive to said pattern is removed thereby uncovering a corresponding portion of said insulating film, and etching said uncovered portion of said insulating film.

12. A method according to Claim 1 which further comprises depositing a second epitaxial high T_c metal oxide superconductor film layer as in paragraph (a) of Claim 1.

13. A method according to Claim 12 which further comprises patterning said second metal oxide superconductor film using a photolithographic process.

14. A method according to Claim 13 wherein said step of patterning said second metal oxide

superconducting film comprises coating said insulating film with photoresist, exposing said photoresist with a desired pattern, developing said photoresist so that a portion of said photoresist responsive to said pattern is removed thereby uncovering a corresponding portion of said second metal oxide superconducting film, and etching said uncovered portion of said second metal oxide superconducting film.

15. A method according to Claim 12 wherein said second high T_c metal oxide superconductor films comprises a mixed metal oxide of yttrium, barium and copper.

16. A microelectronic device comprising a substrate; a first superconductor thin film of high T_c metal oxide superconductor material; and a second insulating thin film having at least one hole, said insulating film being comprised of a material havi- high resistivity at temperatures below T_c, and having a microstructure which is epitaxial or highly oriented sufficient to support epitaxial growth thereon of a third layer.

17. The device according to Claim 16 wherein said insulating film is selected from the group consisting of $SrTiO_3$, yttrium stabilized zirconia, magnesium oxide, lanthanum aluminate, praseodymium barium copper oxide, and yttrium oxide.

18. The device according to Claim 16 wherein said high T_c metal oxide superconductor film comprises a mixed metal oxide of yttrium, barium and copper.

19. The device according to Claim 16 further comprises a third metal layer wherein said third metal layer makes electrical contacts with said first superconductor thin film through said hole.

20. The device according to Claim 16 further comprises a second superconductor thin film of high T_c metal oxide superconductor material wherein said second superconductor thin film makes contacts with said first

superconductor thin film through said hole.

21. The device according to Claim 20 wherein said high T_c metal oxide superconductor film comprises a mixed metal oxide of yttrium, barium and copper.

22. The device according to Claim 16 further includes a plurality of layers deposited within said hole.

23. The device according to Claim 22 wherein said layers comprises a first superconductor layer in contact with said first superconductor thin film, a second insulating layer on top of said first superconductor layer, and a third superconductor layer on top of said second insulating layer.

24. The device according to Claim 22 wherein said layers comprises a first superconductor layer in contact with said first superconductor thin film, a second layer of metal on top of said first superconductor layer, and a third superconductor layer on top of said second layer of metal.

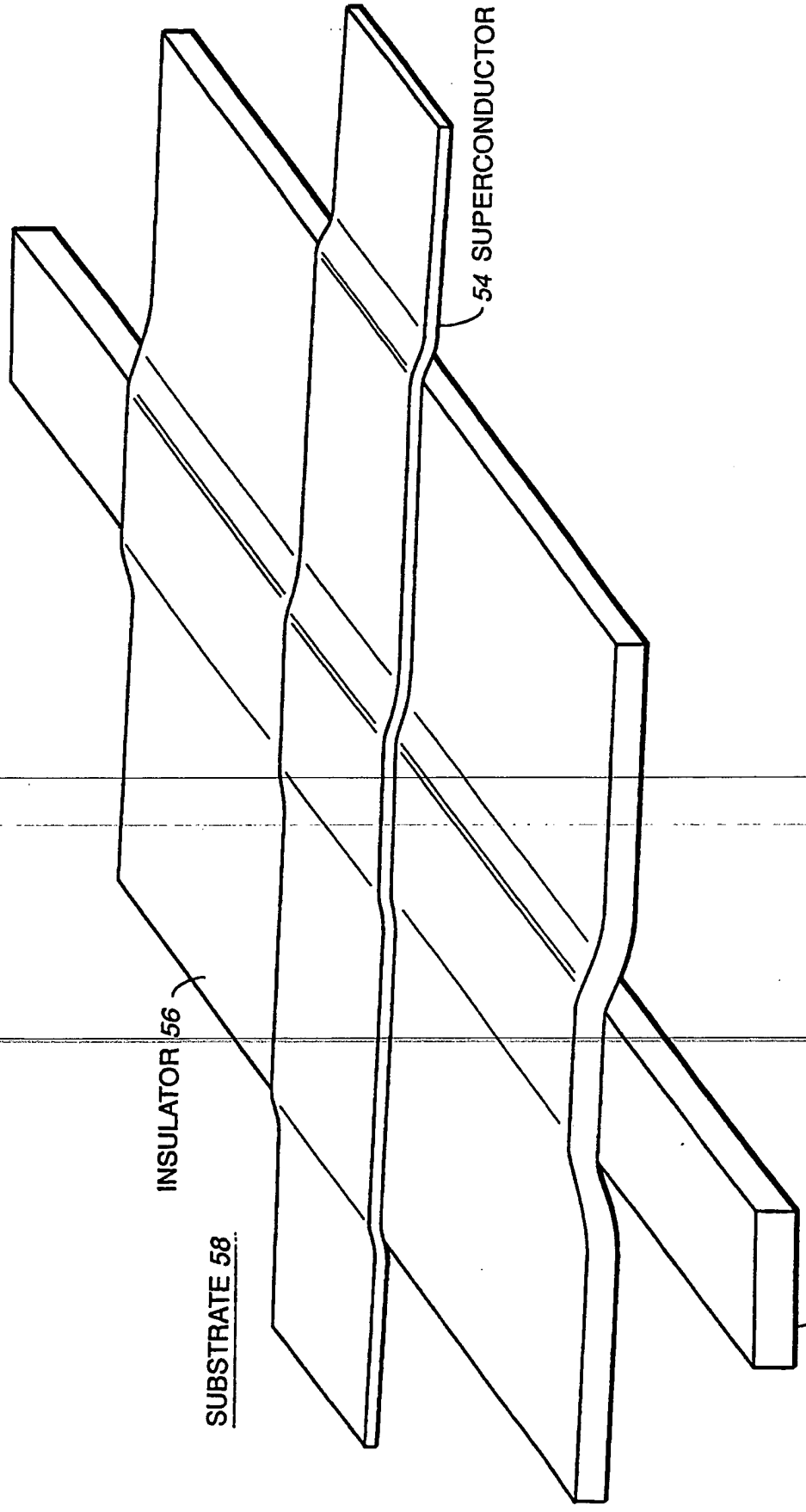

54 SUPERCONDUCTOR
INSULATOR 56
SUBSTRATE 58
52 SUPERCONDUCTOR

FIG._1

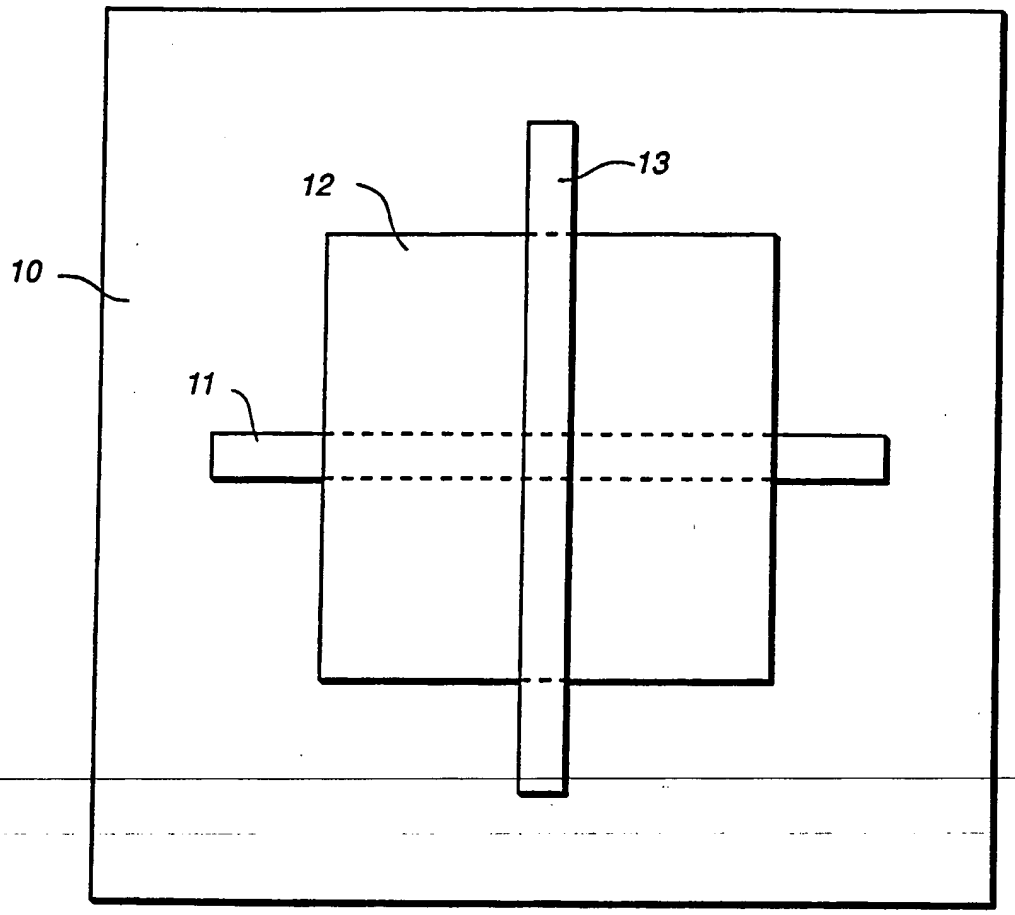


FIG._2A

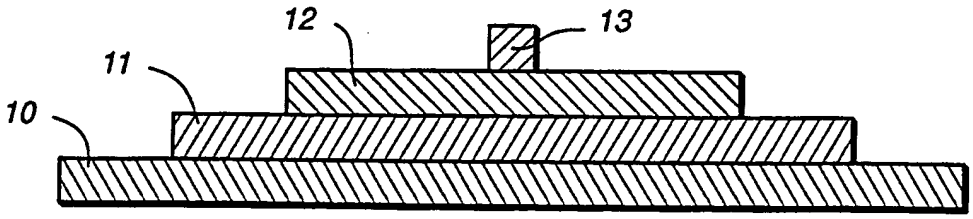


FIG._2B

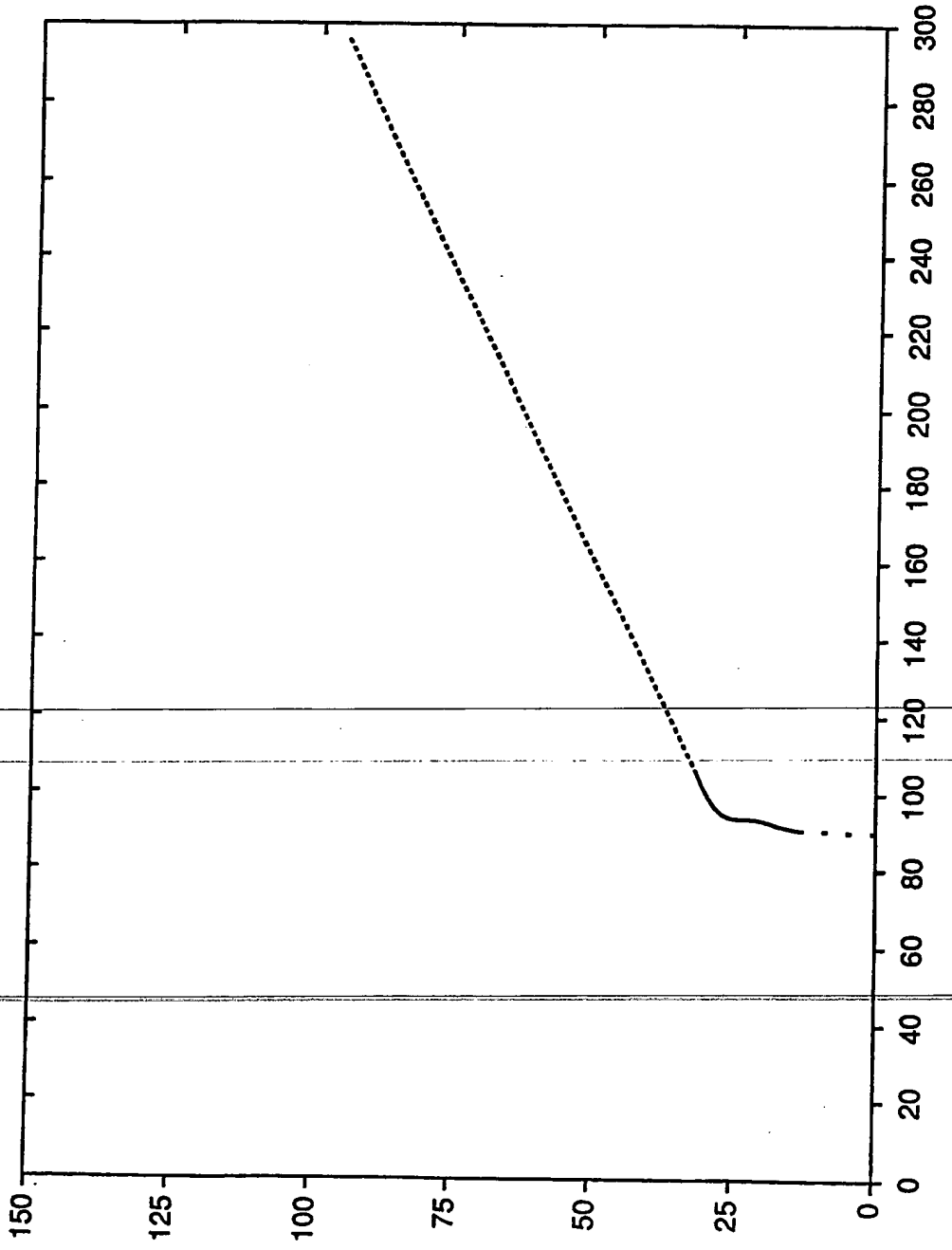

RESISTANCE (OHMS)
150
125
100
75
50
25
0
TEMPERATURE (K)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

FIG._3A

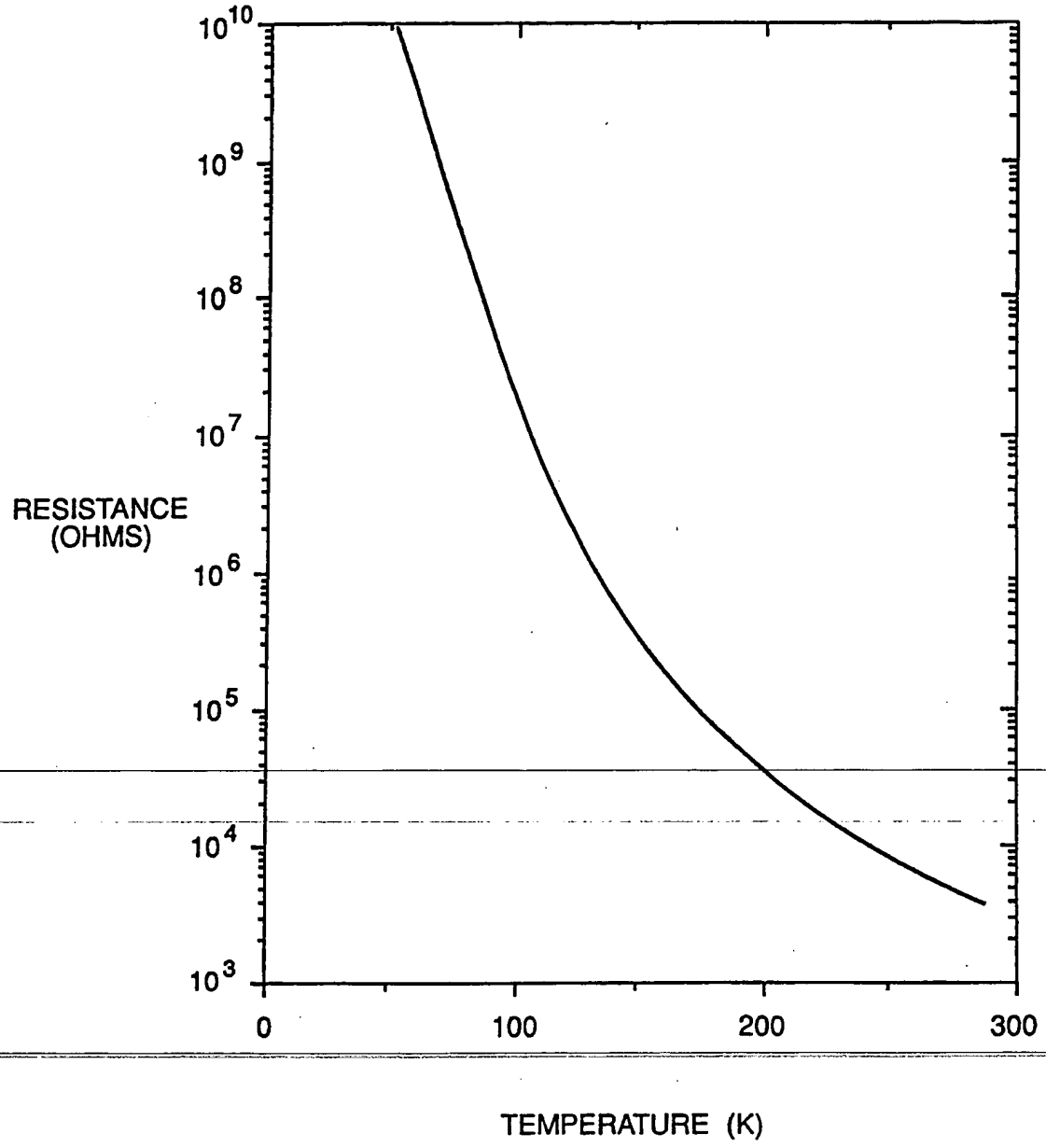

10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
RESISTANCE (OHMS)
0
100
200
300
TEMPERATURE (K)

FIG._3B

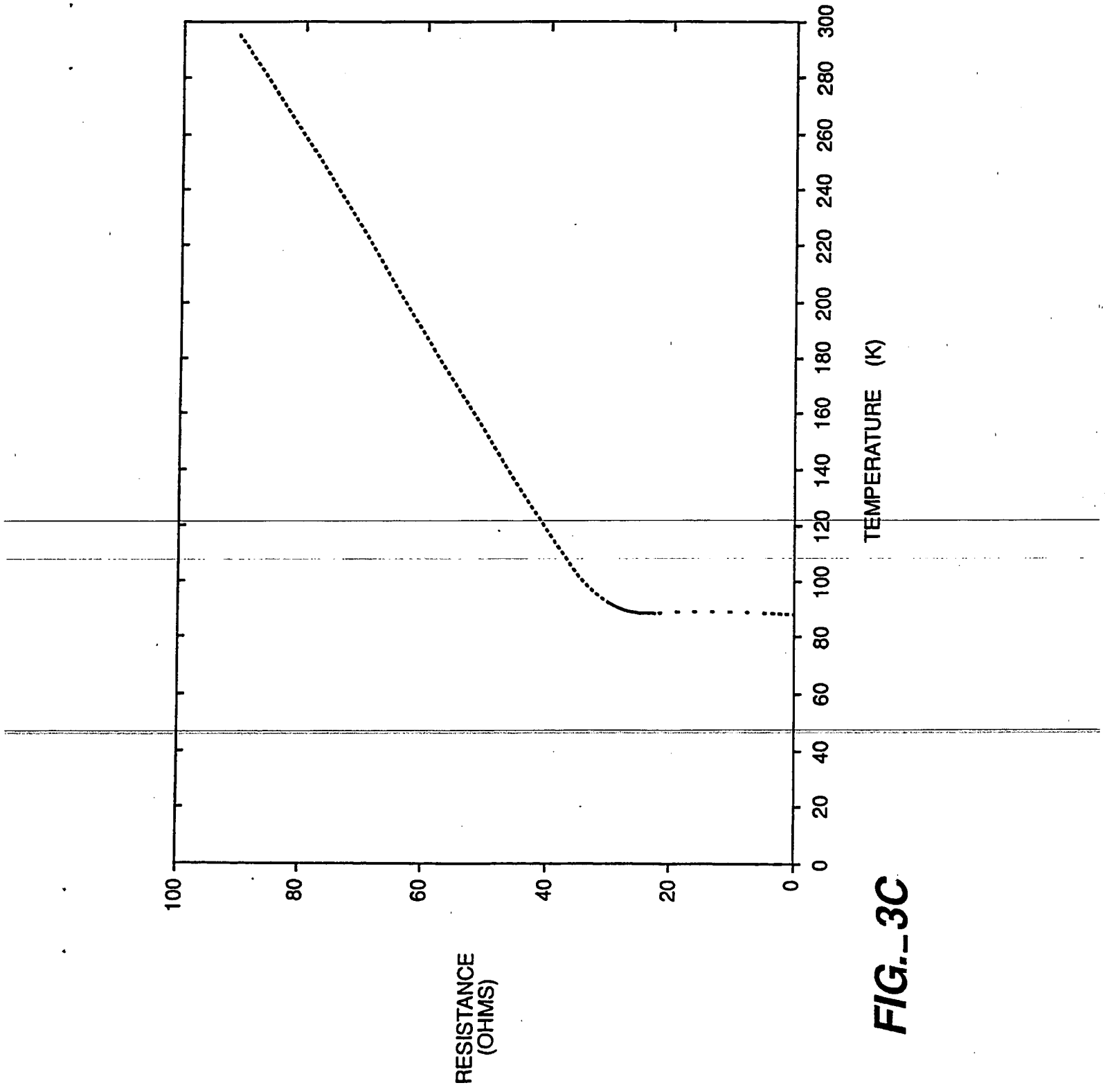

RESISTANCE (OHMS)
100
80
60
40
20
0
TEMPERATURE (K)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

FIG._3C

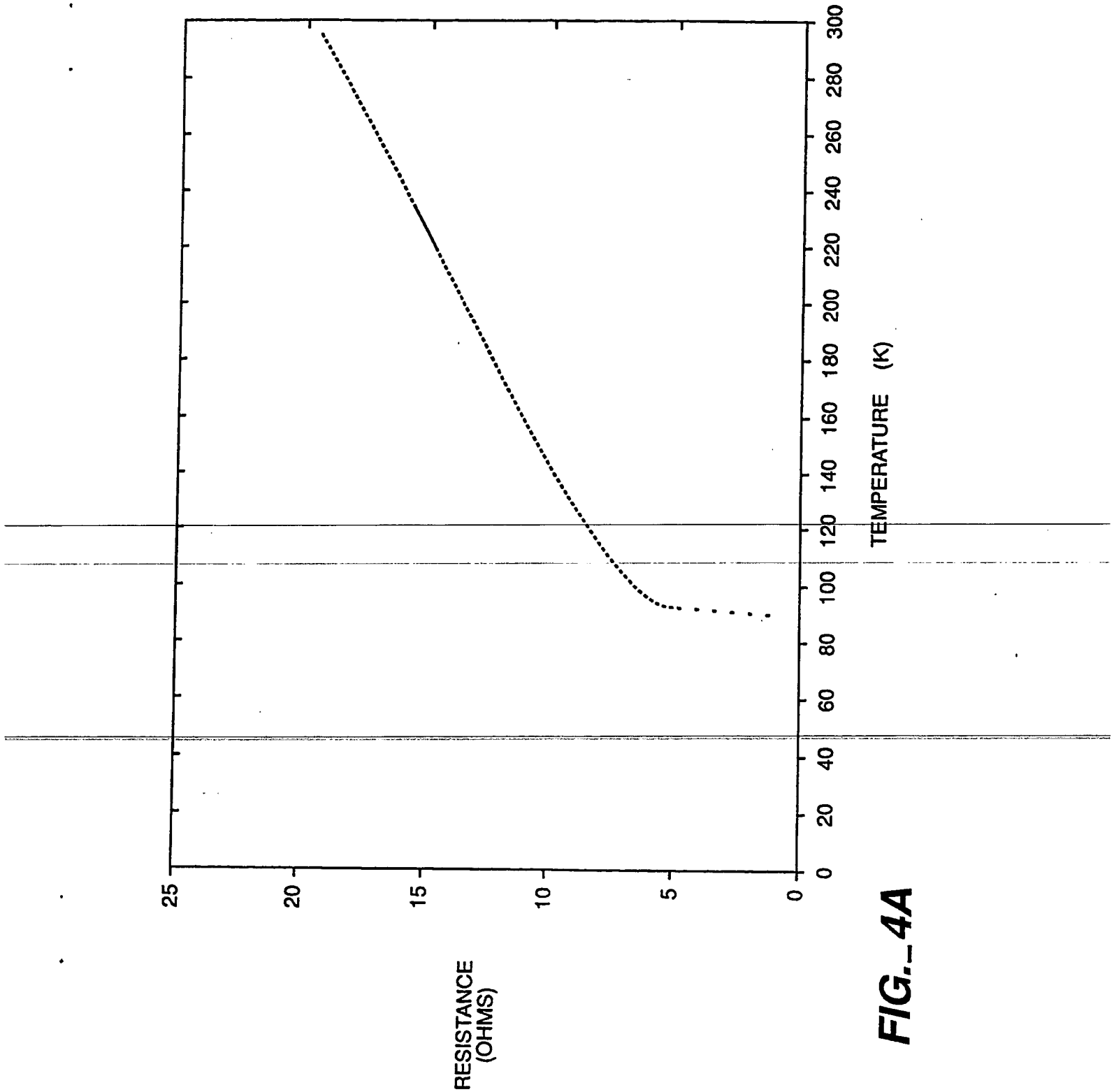

RESISTANCE (OHMS)
25
20
15
10
5
0
TEMPERATURE (K)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

FIG._4A

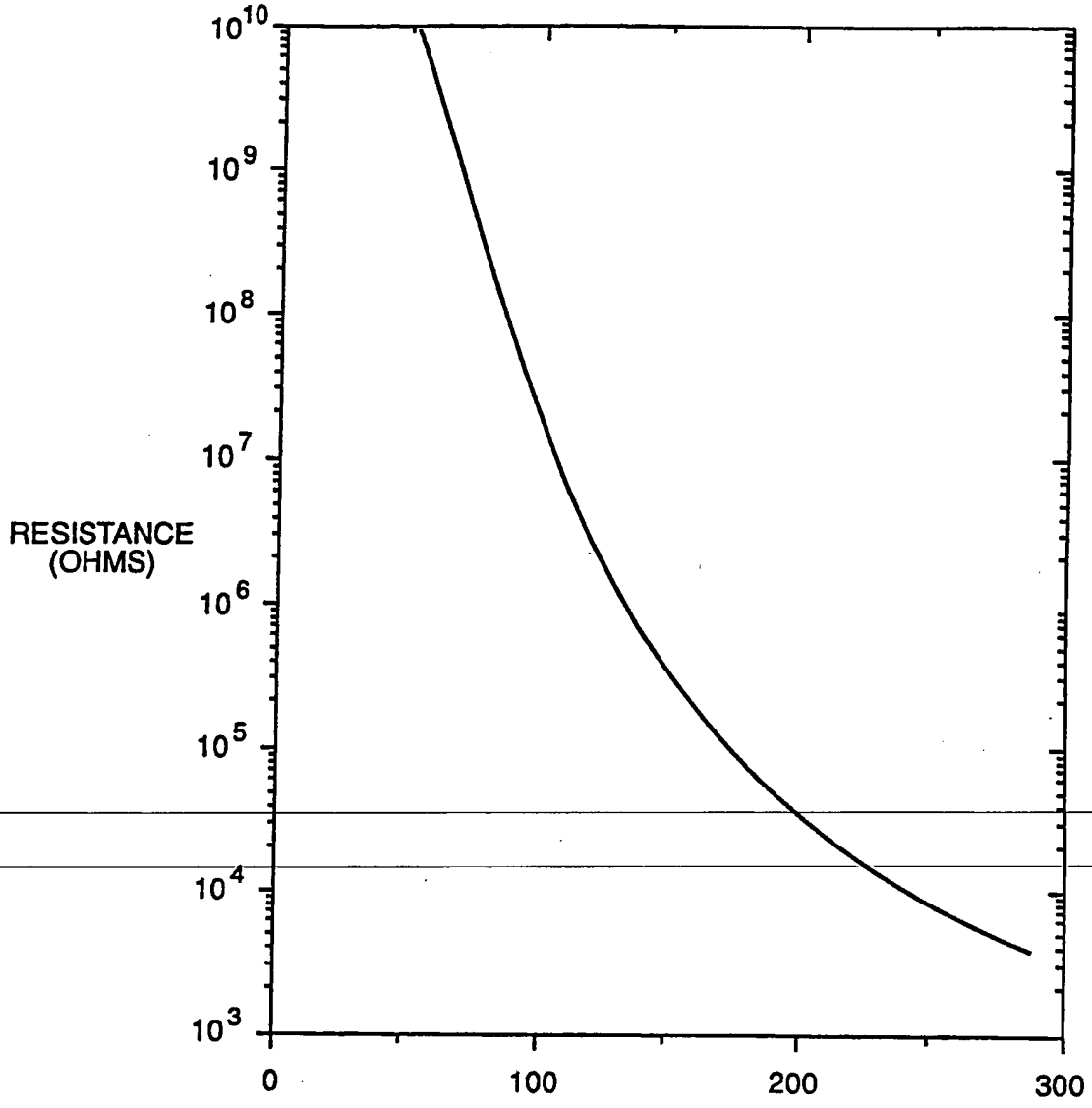

10^{10}
10^{9}
10^{8}
10^{7}
10^{6}
10^{5}
10^{4}
10^{3}
RESISTANCE (OHMS)
0
100
200
300
TEMPERATURE (K)

FIG._4B

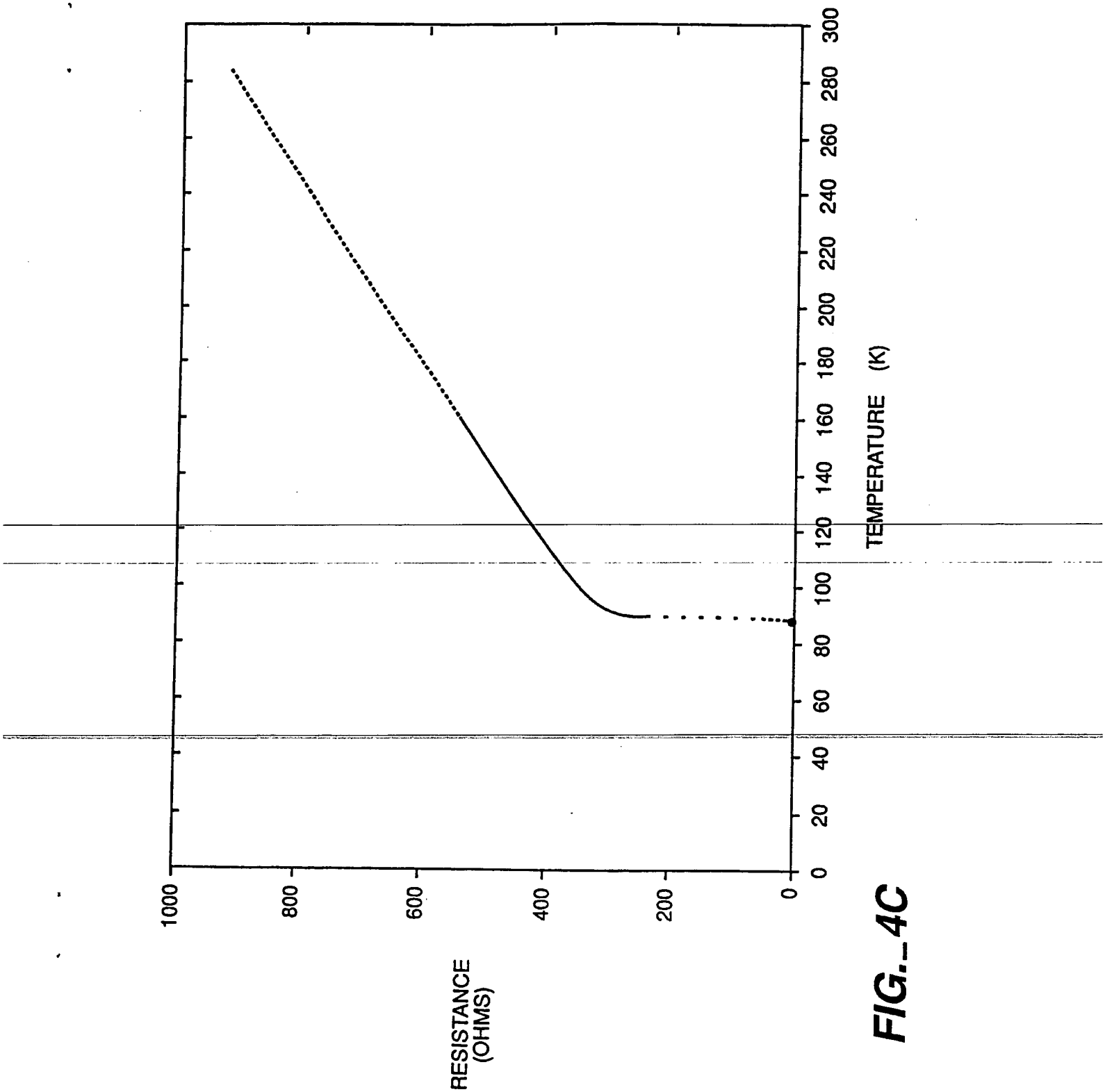

RESISTANCE (OHMS)
1000
800
600
400
200
0
TEMPERATURE (K)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

FIG._4C

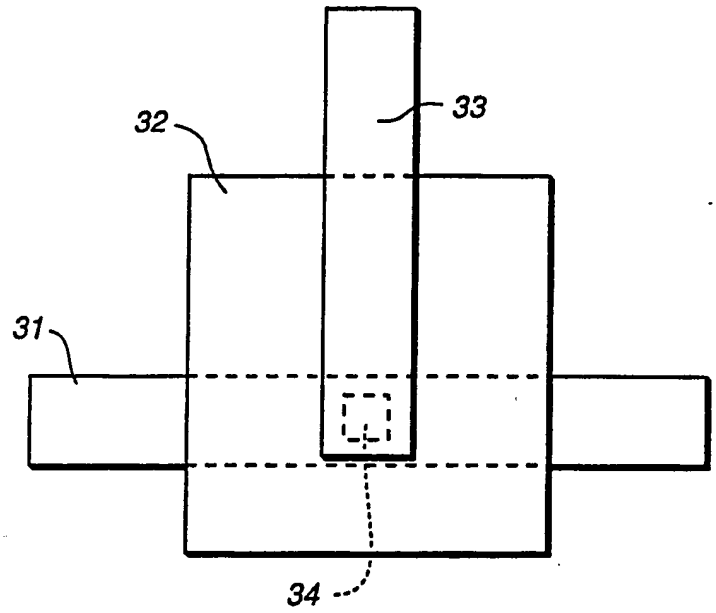


FIG._5A

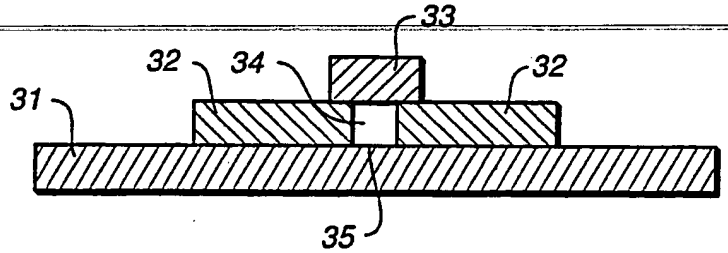


FIG._5B

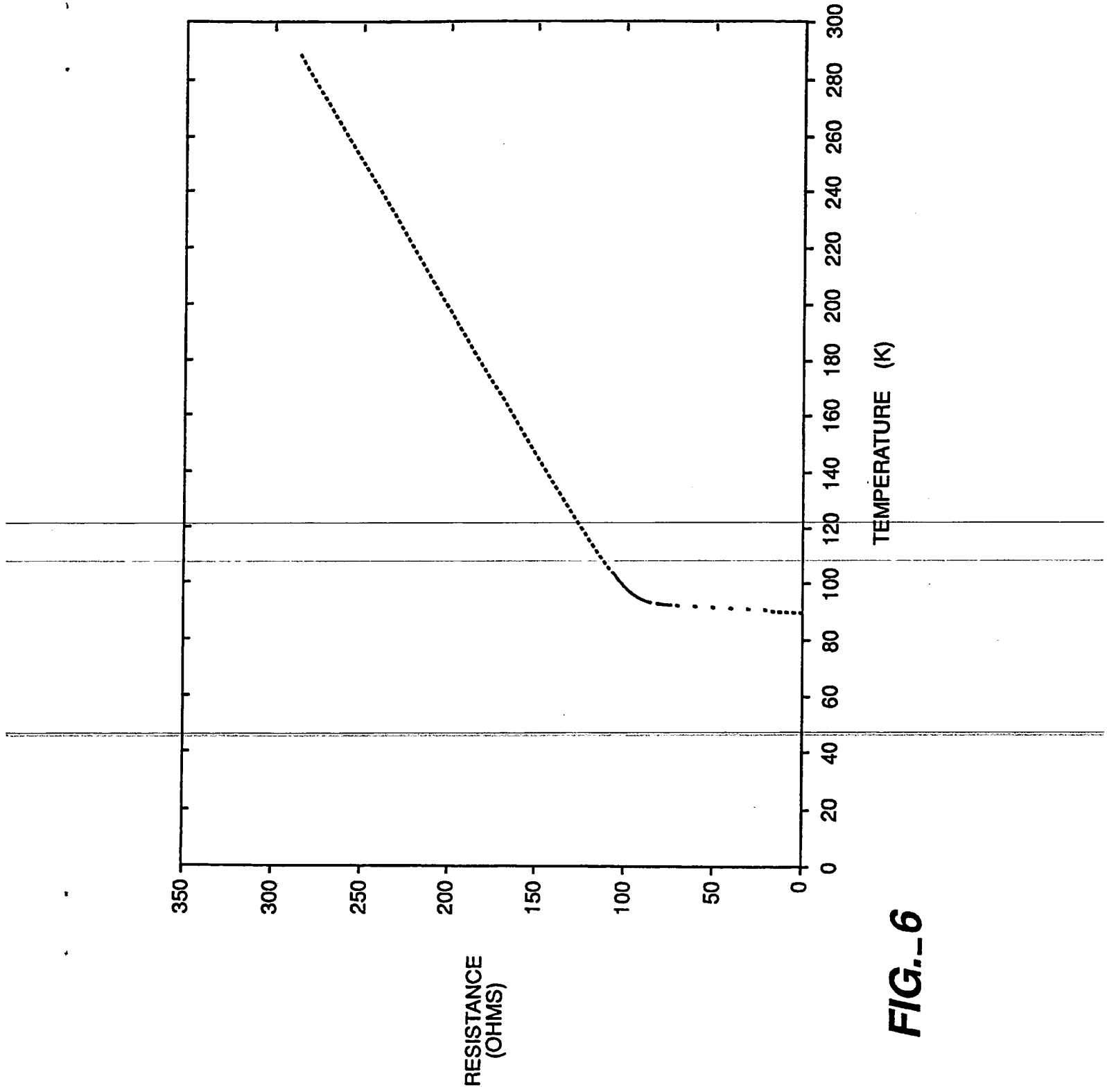

RESISTANCE (OHMS)
350
300
250
200
150
100
50
0
TEMPERATURE (K)
0
20
40
60
80
100
120
140
160
180
200
220
240
260
280
300

FIG._6

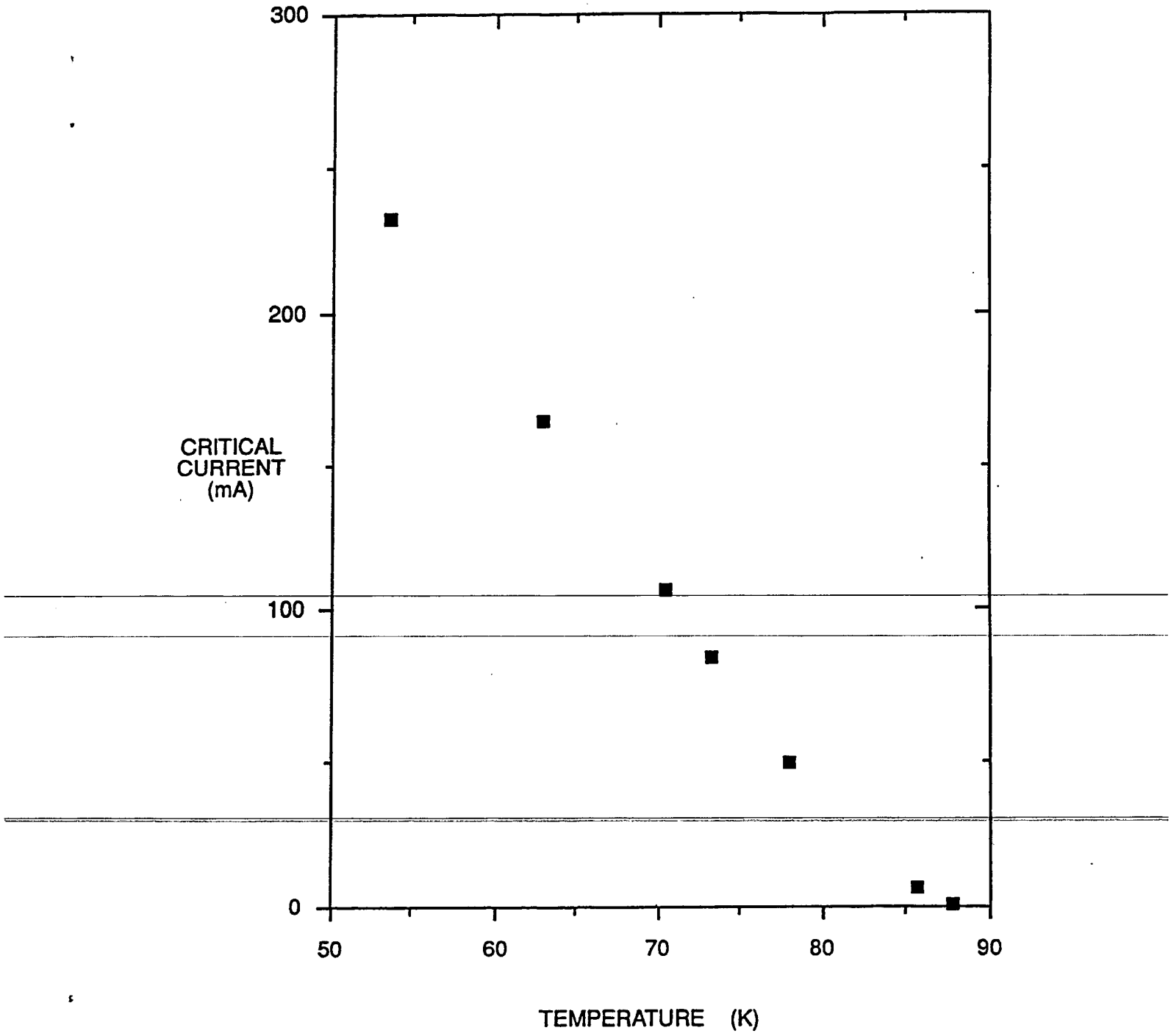


FIG._7

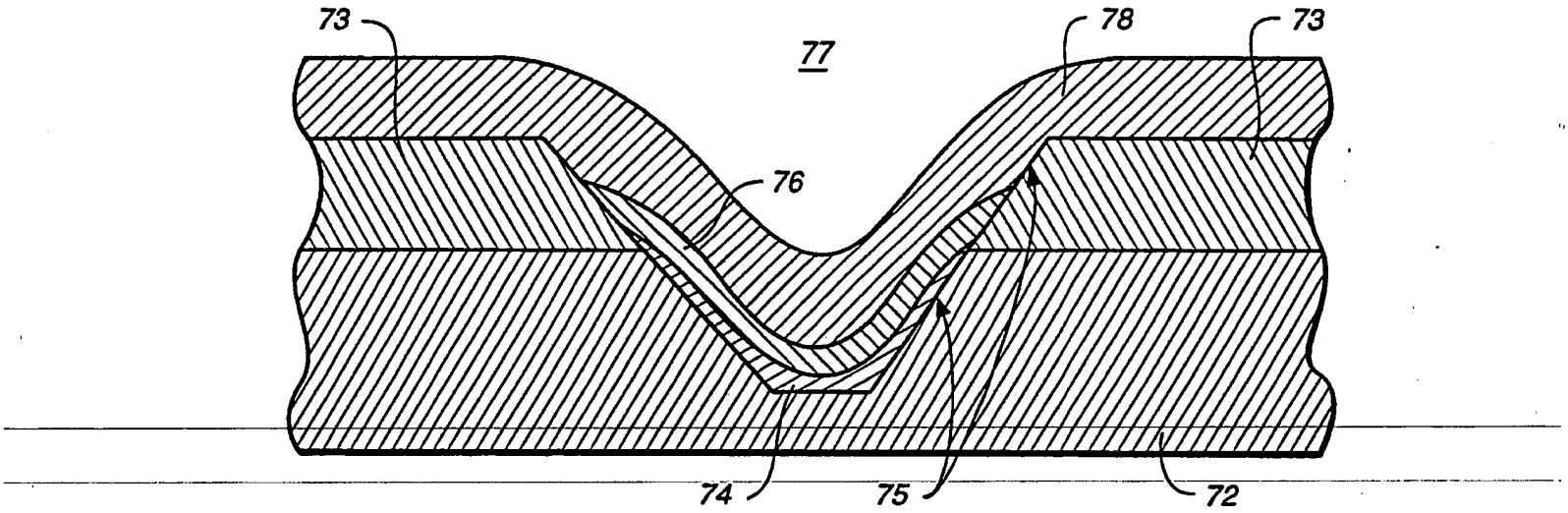


FIG._8

INTERNATIONAL SEARCH REPORT

International Application No. PCT/US91/06812

I. CLASSIFICATION OF SUBJECT MATTER (if several classification symbols apply, indicate all) [6]

According to International Patent Classification (IPC) or to both National Classification and IPC

IPC(5): H01L 39/22, B05D 5/12
U.S. CL. 357/5, 428/930, 427/62,63, 505/1

II. FIELDS SEARCHED

Minimum Documentation Searched [7]

Classification System	Classification Symbols
U.S.	357/5, 428/930 427/62, 63, 505/1,702,728

Documentation Searched other than Minimum Documentation to the Extent that such Documents are Included in the Fields Searched [8]

III. DOCUMENTS CONSIDERED TO BE RELEVANT [9]

Category *	Citation of Document, [11] with indication, where appropriate, of the relevant passages [12]	Relevant to Claim No. [13]
Y	JP, A, 63-283,086, 18 November 1988 (See Abstract)	1,8,9,12,15 16-18,20,21
Y	Appl. Phys. Lett., Volume 53(26), Issued December 1988, R. Vasquez et al, 'Nonaqueous Chemical etch for $YBa_2Cu_3O_{7-x}$' (see pages 2692-2694)	1,3,4,5
Y	US, A, 5,041,188, Myrosznyk et al, 20 August 1991 (See whole document)	1,2,6,7,10-14
Y	JP, A, 02-186,682, 20 July 1990 (See Abstract)	1,2,6-16,18,22
Y	JP, A, 57-30390, 18 February 1982 (See Abstract)	1,16,19,20

* Special categories of cited documents: [10]

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

IV. CERTIFICATION

Date of the Actual Completion of the International Search	Date of Mailing of this International Search Report
20 December 1991	10 JAN 1992
International Searching Authority	**Signature of Authorized Officer**
ISA/US	Roy V. King

Form PCT/ISA/210 (second sheet) (Rev.11-87)

FURTHER INFORMATION CONTINUED FROM THE SECOND SHEET

Y	EP, A1 0329507, 23 August 1989 (See Abstract)	1, 16, 18, 22-24

V. ☐ OBSERVATIONS WHERE CERTAIN CLAIMS WERE FOUND UNSEARCHABLE [1]

This international search report has not been established in respect of certain claims under Article 17(2) (a) for the following reasons:

1. ☐ Claim numbers . because they relate to subject matter [12] not required to be searched by this Authority, namely:

2. ☐ Claim numbers . because they relate to parts of the international application that do not comply with the prescribed requirements to such an extent that no meaningful international search can be carried out [13], specifically:

3. ☐ Claim numbers_____, because they are dependent claims not drafted in accordance with the second and third sentences of PCT Rule 6.4(a).

VI. ☐ OBSERVATIONS WHERE UNITY OF INVENTION IS LACKING [2]

This International Searching Authority found multiple inventions in this international application as follows:

1. ☐ As all required additional search fees were timely paid by the applicant, this international search report covers all searchable claims of the international application.

2. ☐ As only some of the required additional search fees were timely paid by the applicant, this international search report covers only those claims of the international application for which fees were paid, specifically claims:

3. ☐ No required additional search fees were timely paid by the applicant. Consequently, this international search report is restricted to the invention first mentioned in the claims; it is covered by claim numbers:

4. ☐ As all searchable claims could be searched without effort justifying an additional fee, the International Searching Authority did not invite payment of any additional fee.

Remark on Protest

☐ The additional search fees were accompanied by applicant's protest.

☐ No protest accompanied the payment of additional search fees.